Comparative Study of Si, Ge and InAs based Steep SubThreshold Slope Tunnel Transistors for 0.25V Supply Voltage Logic Applications

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With the continued miniaturization of MOSFETs, the OFF-state leakage current (I_{OFF}) is exponentially increasing due to the nonscalability of the threshold voltage imposed by the fundamental 60 mV/decade subthreshold swing at room temperature. This limits the on current (I_{ON}) and the I_{ON}-I_{OFF} ratio severely as the supply voltage is reduced. Interband tunnel transistor [1] features sub-60mV/dec subthreshold slope operation and can be used to circumvent this limitation. This paper examines the potential of double gate (DG) inter-band tunnel FETs (TFET) in 3 different material systems, Si, Ge and InAs, for logic circuit applications down to 0.25V supply voltage (V_{CC}). Based on two-dimensional numerical drift-diffusion simulations [2], we show that 30nm gate length (L_G) InAs (indium arsenide) based TFETs can achieve I_{ON}/I_{OFF} of >$4x10^4$ with <1 ps intrinsic delay at 0.25V V_{CC}. The key features of the InAs TFETs are: a) asymmetric source drain design to suppress the ambipolar leakage b) use of a lower dielectric constant gate oxide (non high-K) and c) high source side injection velocity at moderate electric fields.

The n-channel DG TFETs and MOSFETs used in this study have an L_G of 30 nm and 2.5 nm thick SiO_2 or HfO_2 gate dielectrics. The typical body thickness (T_{body}) is kept at 7 nm. Gaussian doping profiles with doping gradients of 2nm/decade are used for the source and drain regions. Despite the steep subthreshold slope and the I_{ON}-I_{OFF} ratio spanning 12 decades over 1V V_{GS} swing, Si DG TFET I_{ON} (105µA/µm) is much less than Si DG MOSFET I_{ON} (2.27mA/µm) due to the poor tunneling rate of source side valence electrons into the channel conduction band (Fig. 2). Narrow gap semiconductors can enhance the source side tunneling rate due to the combined effects of both reduced barrier height and shorter tunneling distance in addition to the reduced tunneling mass. Figure 4-5 compare the I_D-V_{GS} characteristics of the Ge and InAs based DG TFETs with their MOSFET counterparts. Both Ge and InAs DG MOSFETs suffer from increased band to band tunneling at the drain end, which forward biases the source to channel junction and significantly degrades the I_{ON}-I_{OFF} ratio [3]. It's clearly seen that the performance difference between the TFET and the MOSFET is reduced with reducing bandgap and supply voltage of operation. In order to suppress the ambipolar characteristics, we use asymmetric source and drain doping in InAs DG TFETs which exhibits I_{ON}-I_{OFF} ratio of >$4x10^4$ at 0.25 V V_{CC}. To further highlight the differences in carrier transport between conventional MOSFETs and tunnel FETs, we compared the field and velocity profiles in the channel. Due to the higher longitudinal field at the source side, the TFETs have higher source-side injection velocities compared to the MOSFETs. However, the carrier velocities slow down significantly in the TFETs while traversing the channel due to low electric field. Compositional bandgap grading could be harnessed to induce a quasi-electric field to accelerate carriers in the channel and improve I_{ON} in future TFETs. With increasing drain bias in TFETs, the majority of the potential drop occurs in the p+/n+ junction near the source end which causes delayed saturation and pinch-off characteristics in TFETs compared to their MOSFET counterparts. We compared the effect of scaling the electrical gate dielectric thickness (SiO_2 vs HfO_2) on the performance of Si, Ge and InAs TFETs (Fig. 9). While the Si and Ge TFETs show significant percentage increase in drive current with oxide scaling, the InAs TFETs show negligible sensitivity due to the small tunneling barrier and the limited density of states in the channel from the low effective mass and strong quantum confinement effects. This also results in reduced sensitivity of InAs TFETs to supply voltage (and, hence, electric field) scaling for a fixed I_{ON}-I_{OFF} ratio of 10^4 (Fig. 10).

Finally, we compared the device performance of Si, Ge and InAs tunnel FETs for a fixed I_{ON}-I_{OFF} ratio of 10^4 using a benchmarking approach presented in [4]. The InAs and Ge TFETs, show clear advantage in switching delay,τ, as well as in the energy-delay product, EDP, at fixed I_{ON}-I_{OFF} ratio 10^4, as Vcc is progressively scaled. InAs TFETs show the maximum benefit when the supply voltage V_{CC} is scaled aggressively down to 0.25V and this benefit primarily arises from a) efficient tunneling under low electric field and b) higher source-side injection velocity. MOSFETs in this low V_{DD} range do not even meet the I_{ON}-I_{OFF} stipulation. Thus, narrow bandgap semiconductor based DG TFETs provide a promising device option for ultra-low standby and dynamic power high-speed logic circuits operating under quarter volt supply voltages.

References:

[1] Th. Nirschl et.al., IEDM 2004, pp. 195-198
[2] Sentaurus, Ver. Z-2007.3
[3] T. Krishnamohan et.al., IEEE Transactions Electron Devices, 53, 2006 pp. 990.
[4] R. Chau, S. Datta et al., IEEE Transactions on Nanotechnology, 4, no.2, 2005 pp.153

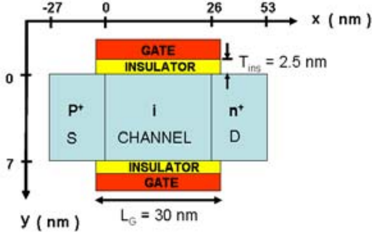

Fig 1a. Simulated Device Schematic

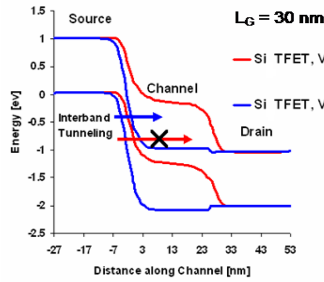

Fig 1b. TFET Operating principle

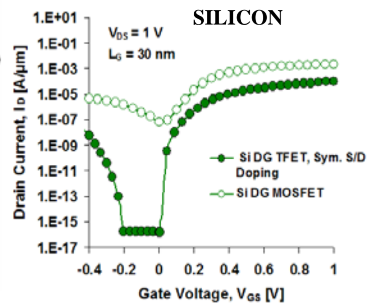

Fig 2. Id-Vg comparison of Si DG TFET v/s Si DG MOSFET

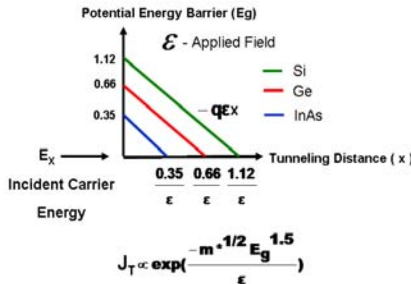

Fig 3. Increased Tunnel Currents for Lower Band Gap and m* materials

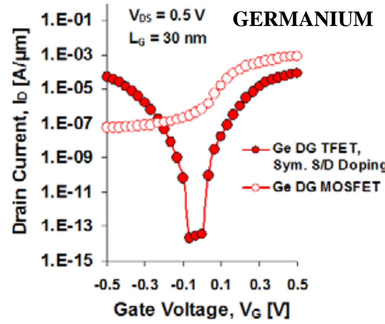

Fig 4. Id-Vg comparison of Ge DG TFET v/s Ge DG MOSFET

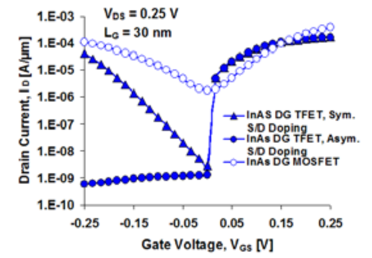

Fig 5. Id-Vg comparison of InAs DG TFET v/s InAs DG MOSFET

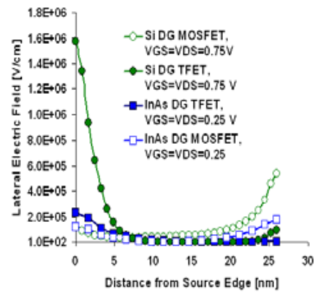

Fig 6. Comparison of Electric Field Profile along the Channel for a TFET v/s MOSFET

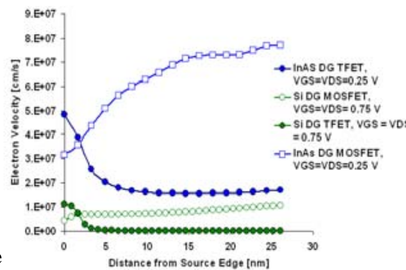

Fig 7. Comparison of Velocity Profile along the Channel for a TFET v/s MOSFET

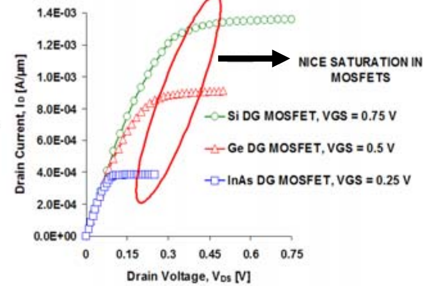

Fig 8a. Id-Vd graph for DG MOSFETs with excellent saturation region

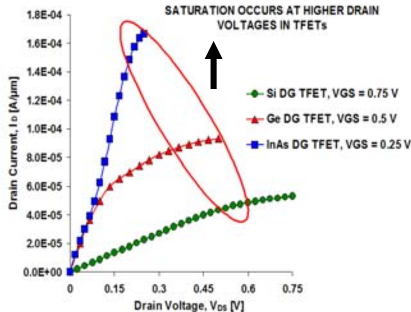

Fig 8b. Id-Vd graph for a Si DG TFET with delayed saturation region

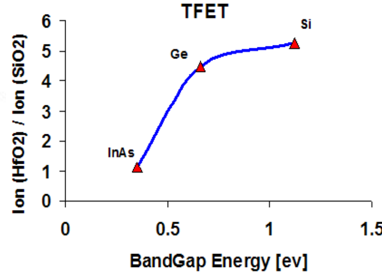

Fig 9. Comparison of the effect of oxide scaling on TFET performance for different materials

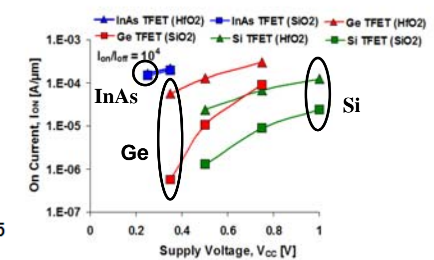

Fig 10. Scaling of On current with Supply Voltage for TFETs in different materials

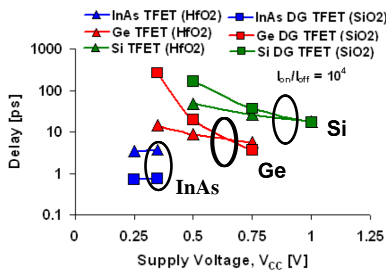

Fig 11. Intrinsic Delay v/s Supply Voltage

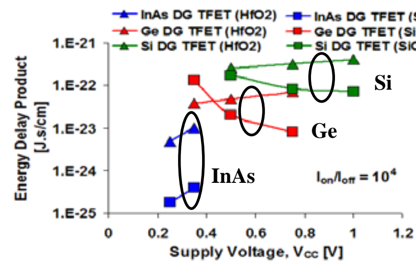

Fig 12. Energy Delay Product v/s Supply Voltage